27.3 A Continuous-Adaptive DDR2 Interface with Flexible Round-Trip-Time and Full Self Loop-Backed AC Test

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As today's multimedia applications require high-performance signal processing, there is a demand for extremely high-bandwidth memory interface [1] on SoC. The DDRx [2] interface has become the most popular memory interface for cost-effectively implementing high-bandwidth and stable parallel transmission. The key circuit techniques of DDRx are the suppression of skew and the wide range of round trip time. In this work, to improve these key features, impedance calibration circuits (ICC) and the flexible round-trip (FRT) circuits for DDRx interface are proposed. The ICC for the SSTL I/O with the look-up table (LUT) and the rising-edge data transmission method are robust to PVT variations and reduce the timing skew among the parallel DQ signals from 165ps to 65ps. The impedance of output drivers are programmable over a wide range by selecting the optimum impedance (18 to 50Ω) with a LUT in the ICC corresponding to each output load condition for any combination of packages and print boards. The DQS round-trip-time in *n*-bits burst read operation is expanded up to *n*/2 cycles of system clock by a dual-FIFO re-synchronization circuit in the FRT. The self loop-backed AC tests [3,4] for test cost reduction by an all-digital DLL are also proposed. In this work, an experimental chip for a 32b DDR2 SDRAM interface for SoC is fabricated in 90nm CMOS and achieves 960Mb/s/pin operation.

The overall view of DDR2 SDRAM interface designed for SoC application is shown in Fig. 27.3.1. The purpose of this circuit is to reduce the timing skew from the system clock to the SSTL output in DQS and DQs for stable high-speed transmission. For this timing skew reduction, we use two kinds of DLLs. One is a master that generates codes for one clock cycle delay (360˚). Others are slaves that receive 90/270˚ delay codes calculated from 360˚. Some of slave DLLs generate an output clock to the SDRAM shifted by 90/270˚. The rest of the slaves DLLs are used for the data read operation from SDRAM. PVT variations are the major cause of timing skew in DQS and DQs, degrading the performance. In this master-slave DLL architecture, only the system clock rising edge is used for timing generation, such as 90/270˚ clock signals, in order to eliminate clock duty imbalance,. This rising clock edge method is also used in SSTL output buffers. FFs receive alternately 90/270˚ clock signals and update the states of multiplexers (MUX) A and B in Figure 27.3.1, which has four states: high impedance (Hi-Z), H/L data output (Data H/L) and on-die termination (ODT) on. There are two level shifters from 1.0V to 1.8V in SSTL output buffer. The one connected to the pull-up driver receives the signal from A of MUX and the other connected to pull-down driver receives the signal from B. Switching of both of pull-up and pull-down drivers is triggered only by the rising signal edge. Furthermore, the timing skew of SSTL output is lowered with impedance calibration for output driver.

Figure 27.3.2 shows the impedance calibration circuit (ICC) for SSTL output. This ICC consists of 15kΩ off-chip reference resistance, voltage comparator, binary-search circuit and LUT. In the calibration sequence, the first step is to adjust the current of the reference transistor to 60μA. The second step is to transfer the gate voltage of the reference transistor to the unit transistors. The third step is to search the number of unit transistors to be turned-on to balance their current with the output transistor current by binary search method. The final step is to refer to the LUT to determine the number of output transistors to be turned on from the results of the third step. With this calibration, which runs during SDRAM auto-refresh operation, the PMOS and NMOS output driver impedance is adjusted precisely in a very short period of 8 clock cycles and the timing skew is kept small. Additionally, the LUT is programmable to allow selecting impedance values for suitable SSTL switching performance for various kinds of packages and printed board design combinations.

To achieve high frequency operation, it is not enough to reduce the timing skew. As the clock cycle time is getting shorter, the round-trip-time of DQS becomes longer than one clock cycle. DQS round-trip-time is the time from system clock rising edge in SoC to the arrival of DQS at input PAD of SoC from SDRAM. In conventional DDR-SDRAM interface circuit design, it is difficult to operate with DQS round-trip-time longer than one clock cycle and various in each byte-lane. The DDR SDRAM interface circuit proposed in this paper has the capability to allow various DQS round-trip-time up to *n*/2 cycles in *n*-bits burst operation. In this circuit, dual-FIFOs that operate alternately are used. Figure 27.3.3 shows the operation waveform when data arrives from SDRAM after *n*/2-0.5 cycle round-trip-time. From the figure, fifo_d0 receives the first burst data set, then fifo_d1 receives the second burst data set. To allow longer DQS round-trip-time, high-impedance period of DQS between burst read operations can be managed properly. After the first write operation to fifo_d0, a false pulse in the 'Write Point Reset' signal may be generated during this high-impedance period. To avoid overwriting data on fifo_d0, this false pulse is masked not to propagate to fifo_d0. This false pulse propagates to fifo_d1. However, in our circuit, next correct reset pulse is given and write operation to fifo_d1 can be done properly.

In this work, a self loop-backed method is applied to measure AC parameters such as setup and hold time and using a low-frequency and low-cost tester. To guarantee the high-speed DDR SDRAM interface operation, all of the AC parameters shown in Fig. 27.3.4 must be measured. With this method, a measurement resolution of about 80ps is achieved at 800Mb/s operation on a low-speed tester. This 80ps corresponds to 1/32 of one cycle time of 2500ps that is controlled by DLL and delay code generator.

Figure 27.3.5 shows the measurement scheme for setup/hold time (t_{WDS}/t_{WDH}) of DQ to DQS output and clock duty of DQS (t_{WDQSH}/t_{WDQSL}). In normal operation, the DLL and delay code generator are used for 90/270˚ clock and those timings are continuously updated. In the AC parameter test for setup/hold time, the same circuit changes clock timing to the testing point that is shifted from 90/270˚ timing. The clock duty of DQS is measured by using the variable delay line and the digital phase detector in the DQS preamble detection circuit. For this testing, the necessary functions of tester are signal termination and expected value comparison at the operation frequency of 10MHz.

Figure 27.3.6 shows a variety of test measurement data. Figure 27.3.6(a) shows V_{DD} versus data-rate plot. An experimental chip operates at 960Mbps/pin on a board with 4 DRAMs ×8 DQ. Figure 27.3.6(b) shows a micrograph of the implementation board. Fig.27.3.6(c) shows the waveform of DQS and DQ in write operation at 800Mb/s. Fig.27.3.6(d) shows a micrograph of an experimental chip fabricated in 90nm CMOS 7Cu process. 1.8V is supplied to SSTL I/O and 1.0V is supplied to the core area.

References:

[1] Y. Tokunaga, S. Sakiyama, et al., "A 0.03mm² 9mW Wide-Range Duty-Cycle Correcting False-Lock-Free DLL with Fully Balanced Charge-Pump for DDR Interface," *ISSCC Dig. Tech. Papers*, pp. 330-331, Feb., 2006.

[2] H. Fujisawa, S. Kubouchi, et al., "An 8.4ns Column-Access 1.3Gb/s/pin DDR3 SDRAM with an 8:4 Multiplexed Data-Transfer Scheme," *ISSCC Dig. Tech. Papers*, pp. 162-163, Feb., 2006.

[3] M. Tripp, T.M. Mak, and A. Meixner, "Elimination of Traditional Functional Testing of Interface Timing at Intel," *Int. Test Conf.*, pp. 1014-1022, Sep., 2003.

[4] B. Provost, T. Huang, C.H. Lim, et al., "AC IO Loopback Design for High Speed μProcessor IO Test," *Int. Test Conf.* pp. 23-30, Oct., 2004.

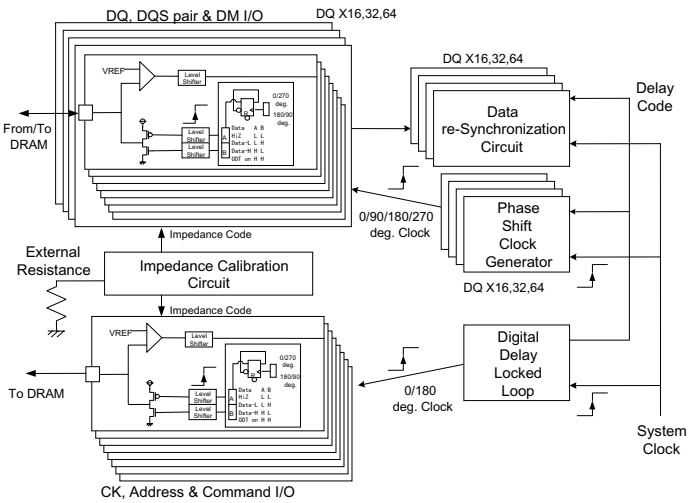

Figure 27.3.1: Overall view of DDR interface.

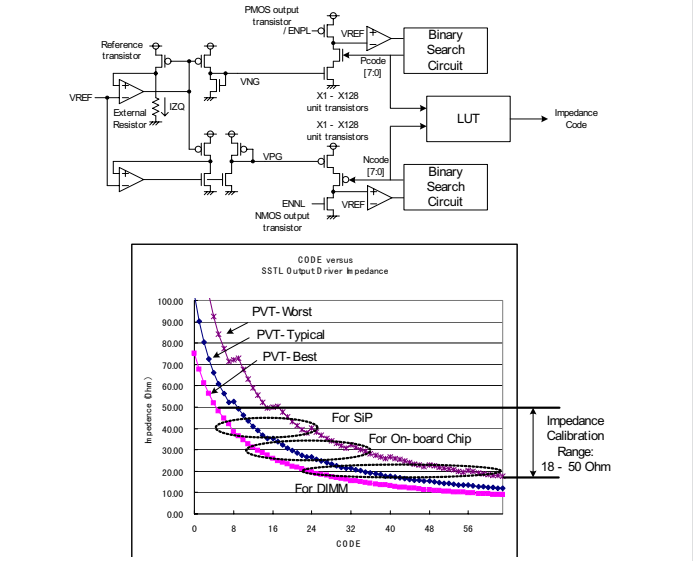

Figure 27.3.2: SSTL I/O output driver impedance calibration.

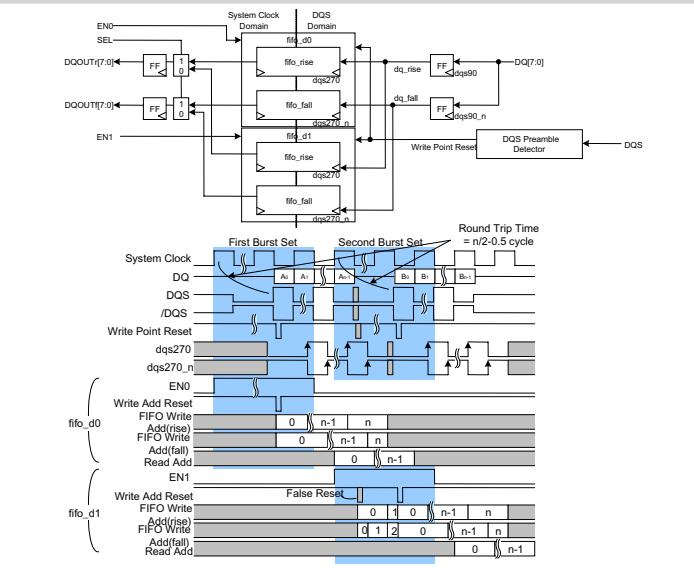

Figure 27.3.3: Diagram of n-bits burst operation of dual-FIFO scheme.

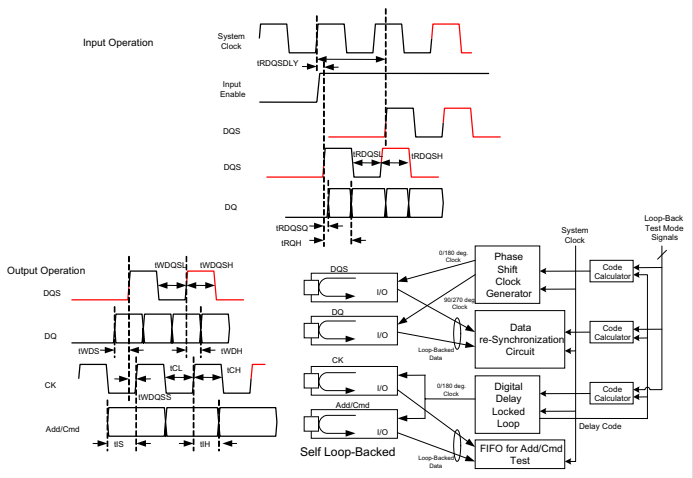

Figure 27.3.4: AC measurement parameters for DDR interface operation.

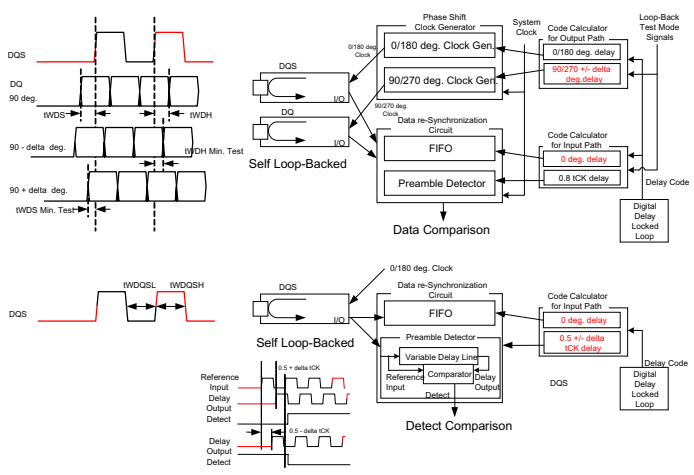

Figure 27.3.5: Circuit diagram of AC loop-backed test method.

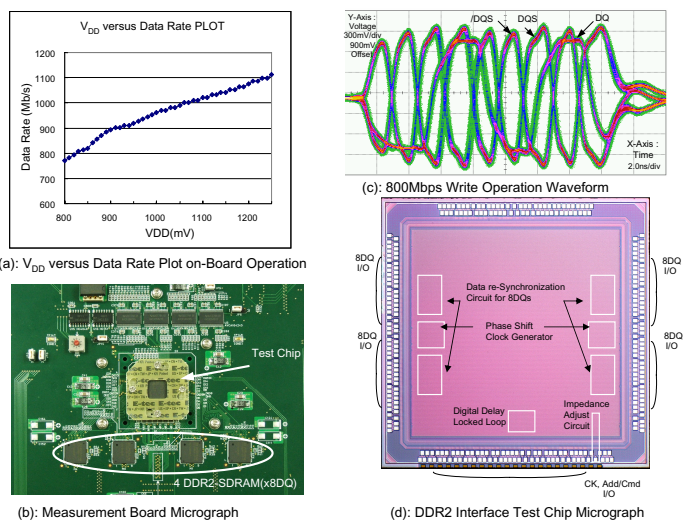

Figure 27.3.6: Test chip measurement results.